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APPLICANT: Theus et al.

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EXAMINER: n/a

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
W	A	5,477,186	12/19/95	Kobatake	330	9	8/5/94
W	B	5,745,002	4/28/98	Baschiroto et al.	327	554	10/19/94
W	C	6,259,316	7/10/01	Nagaraj	330	9	5/12/99
	D						
	E						
	F						
	G						
	H						

**FOREIGN PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
	I						YES-abstract
	J						
	K						
	L						
	M						

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL		
W	N	Pierre Favrat et al., "A High-Efficiency CMOS Voltage Doubler," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 33, No. 3, March 1998, pages 410-416.
W	O	Gerrit W. den Besten et al., "Embedded 5 V-to-3.3 V Voltage Regulator for Supplying Digital IC's in 3.3 V CMOS Technology," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 33, No. 7, July 1998, pgs. 956-962.
EXAMINER	NGUYEN, KW	
	DATE CONSIDERED	12/09/04

**EXAMINER:** Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.